



Gp/2811

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Wendell P. Noble et al.

Title: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR

Docket No.: 303.379US2
Filed: April 17, 2000
Examiner:

Serial No.: 09/551,027
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Group Art Unit: 2811

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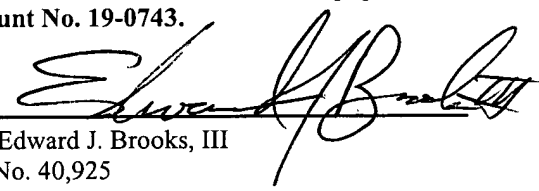
Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

- X A return postcard.
- X A Supplemental Information Disclosure Statement (1 pgs.), Form 1449 (1 pgs.), and copies of 7 cited references.

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 21 day of December, 2000.

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